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Official PATENT

circuitry for disabling the clock enable signal if the estimated total bandwidth utilization for the controllers accessing the memory controller is zero; and

circuitry for disabling the memory clock responsive to the disabling of the clock enable signal.

34. (Twice Amended) The system of claim 20, wherein the circuitry for selecting one of the plurality of clocks for the resource responsive to the estimated total bandwidth utilization comprises:

a multiplexer having a plurality of inputs for receiving the plurality of clocks and a selection input for receiving a selection value determined in response to the estimated total bandwidth utilized by the zero or more controllers accessing the resource.

5. The system of claim 4, further comprising:

a frequency table in communication with the selection input to the multiplexer and the circuitry for estimating the total bandwidth utilized by the zero or more controllers accessing the resource for outputting the selection value responsive to the estimated total bandwidth utilized by the zero or more controllers accessing the resource.

9. The portable electronic device of claim 23, further comprising:

a frequency table having entries describing clock frequencies for a resource in the portable electronic device, wherein the sum produced by the clock controller is an index to an entry in the frequency table.

10. The portable electronic device of claim 23, wherein the clock controller further comprises:

a multiplexer for receiving the plurality of clocks generated by the clock generator and outputting a clock selected responsive to the sum of the register values.

11. The portable electronic device of claim 23, further comprising circuitry for applying the selected clock to the resource.

12. The portable electronic device of claim 23, wherein there are a plurality of resources comprising:

a bus for transferring information among ones of the plurality of controllers in communication with the bus;

a memory controller in communication with the bus for controlling access to at least one external memory device by ones of the plurality of controllers; and

a central processing unit controller in communication with the bus for controlling accesses to a central processing unit by ones of the plurality of controllers.

13. The portable electronic device of claim 12, wherein the memory controller communicates with the external memory device using a clock and a clock enable signal and the portable electronic device further comprises:

circuitry for disabling the clock enable signal when the bandwidth utilized by the controllers accessing the memory is zero; and

circuitry for terminating the memory clock when the clock enable signal is disabled.







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17. The method of claim 24, wherein the resource is a memory controller and the determining step determines that zero controllers are accessing the memory controller, further comprising the steps of:

disabling a clock enable signal from the memory controller; and

disabling a clock to the memory controller.

18. An application-specific integrated circuit for processing data, the circuit comprising:

a plurality of programmable registers for holding values, wherein each register is adapted to hold a value describing data processing rate of an associated device;

an adder in communication with the plurality of programmable registers for summing the values in ones of the plurality of registers associated with devices accessing a resource, wherein the sum describes the total data processing rate of the devices accessing the resource; and

selection circuitry in communication with the adder for selecting one of a plurality of clock frequencies for the resource responsive to the sum produced by the adder.

19. The application-specific integrated circuit of claim 18, further comprising:

a frequency table in communication with the adder and the selection circuitry for converting the sum produced by the adder into a selection value for use by the selection circuitry for selecting one of the plurality of clock frequencies.

20. A system for selecting a clock frequency for a resource accessed by zero or more controllers from among a plurality of clocks of different frequencies, the system comprising:





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a plurality of registers, wherein each register is associated with at least one controller capable of accessing the resource and each register is adapted to hold a value describing bandwidth utilized by the at least one associated controller;

circuitry, in communication with the plurality of registers, for estimating the total bandwidth utilized by the zero or more controllers accessing the resource responsive to the values held in the registers; and

circuitry for selecting one of the plurality of clocks for the resource responsive to the estimated total bandwidth utilization.

21. The system of claim 20, wherein the plurality of registers are programmable.

22. The system of claim 20, wherein the circuitry for estimating the total bandwidth utilized by the zero or more controllers comprises:

summing circuitry for summing the values held in registers associated with controllers accessing the resource.

23. A portable electronic device comprising:

a resource for processing data, wherein the rate that the resource processes data is at least partially determined by a frequency of a clock received by the resource;

a clock generator for generating a plurality of clocks having different frequencies;

a plurality of controllers for accessing the resource, wherein each controller is adapted to access the resource at a given bandwidth;

a plurality of bandwidth registers, each bandwidth register associated with a controller and adapted to hold a value representative of the given bandwidth at which the controller accesses the resource; and







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a clock controller adapted to sum the values of the bandwidth registers associated with the controllers accessing the resource and select a clock of the plurality of clocks for the resource responsive to the sum.

24. A method of selecting one of a plurality of clocks having different frequencies for a resource, wherein the clock frequency determines at least in part the bandwidth that the resource can process, comprising the steps of:

determining whether zero or more controllers are accessing the resource;

assigning a value to each controller representative of bandwidth utilized by that controller;

estimating a total bandwidth utilized by the zero or more controllers accessing the resource by summing the values assigned to the controllers that are accessing the resource; and

selecting one of the plurality of clocks responsive to the estimated total bandwidth utilized by the zero or more controllers accessing the resource.

## REMARKS

Claims 1-24 are pending prior to entry of this Amendment. Claims 18-24 are allowed, claims 1, 4-7, and 14 are rejected, and claims 2, 3, 8-13, and 15-17 are objected to. In response, claims 1, 3, 6-8, and 14-16 are canceled, and claim 4 is amended.

Claims 4 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Specifically, the Examiner states that in claim 4, lines 1-2, the phrase, "the circuitry for dynamically and automatically selecting," lacks a proper antecedent basis because its base claim, 20, does not recite "dynamically and automatically." In response, Applicants have amended claim 4 to eliminate the phrase, "dynamically and automatically." As for claim 5, it is dependent on claim 4, which is dependent on independent claim 20. Applicants submit that claim 5 does







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